REMARKS/ARGUMENT

Claims 8 and 10 have been cancelled without prejudice. Claim 1 has been amended to include the limitations of claims 8 and 10. The amendment to claim 1, therefore, does not raise new issues. Entry of the amendment is respectfully requested.

Claim 10 was rejected under 35 U.S.C. §103(a) over Williams, U.S. Patent No. 5,248,627 in view of Kalnitsky, U.S. Patent No. 5,418,174. As basis for the rejection it was set forth that Figures 6 and 7 of Williams show a device which includes an interlayer dielectric with dopant ions. It is respectfully submitted that Figures 6 and 7 of Williams do not show such a feature. If the Examiner disagrees, the applicants' attorneys respectfully ask the Examiner to identify that portion of Williams in which a doped interlayer dielectric layer is shown. Otherwise, it is respectfully submitted that claim 1, which now includes the limitations of claim 10, should be allowable. Reconsideration of claim 1 is requested.

Further, the applicants' attorneys request the consideration of the following points, which have been previously raised.

The Examiner has concluded that Williams teaches all of the limitations of claim 1, including a gate oxide that is less than 1000Å thick and a gate electrode comprised of p-type polysilicon. In the previous papers filed, the applicants' attorneys have maintained that Williams does not teach a p-type gate electrode in combination with a gate oxide that is less than 1000Å thick. That, in fact, Williams teaches away from such a combination. The following excerpt from Williams illustrates the latter point:

> "Another conventional technique for reducing V_{tp} of a PMOS device, one which is useful even in processes having long diffusion times after the polysilicon deposition step, is to use boron-doped p-type polysilicon gates in association with the PMOS devices, instead of phosphorus-doped n-type polysilicon gates. The p-type polysilicon has a different work function, so that the threshold of the PMOS devices is shifted by about a volt. <u>Unfortunately, this technique is not entirely satisfactory for use in processes specifying a thin gate oxide, as the boron from the p-type polysilicon penetrates easily through the thin gate oxide in any subsequent diffusion steps and can counterdope the channel. Leakage and other problems result.</u>" (emphasis added).

Williams does not show a device with a p-type gate electrode and a gate oxide layer that is less than 1000Å thick. Williams mentions the 1000Å thick gate oxide only to explain that the combination of a p-type gate electrode and a gate oxide that is less than 1000Å thick leads to "unsatisfactory" results. Clearly, Williams is discouraging the use of a 1000Å thick gate oxide layer in combination with a p-type gate electrode. Thus, although Williams teaches that a Mosgated device having a p-type gate electrode is possible, it explicitly states that such a device should not have a gate oxide that is less than 1000Å thick. Col. 2, lines 65-68.

However, the Examiner states that Williams teaches using a gate oxide layer that is between 100-1200Å thick. See Office Action dated 11/20/2002, page 7, second full paragraph (citing Col. 4, lines 38-40). In the portions cited by the Examiner, Williams teaches using 100-1200Å thick gate oxide layer in combination with an n-type gate electrode. Given the explicit statements in Williams to not combine a gate oxide layer that is less than 1000Å thick with a p-type gate electrode, it cannot be said that Williams teaches a device with a p-type gate electrode and a gate oxide that is less than 1000Å thick.

In addition, the Examiner has stated that although Williams does not show a radiation hardened gate oxide, the combination of a radiation hardened gate oxide and the teaching of Williams makes the subject matter of claim 1 obvious, in that Kalnitsky teaches the use of a radiation hardened gate dioxide layer. It is respectfully submitted that Kalnitsky does not teach the use of a radiation hardened gate oxide layer that is less than 1000Å thick as called for by claim 1. Furthermore, the use of such a thin layer of radiation hardened gate oxide is not an obvious variation in that thin gate oxides (less 1300Å, see specification at page 3, lines 2-4) are known to lack the ability to withstand SEE, and are thus not generally though desirable for use in space application. However, contrary to this conventional thinking, a thin gate oxide (less than 1000Å) in combination with other features set out in claim 1 has been found by the inventors to have the ability to withstand both high radiation dosage and SEE. (See specification at page 6, lines 13-16) Therefore, having a radiation gate oxide that is less than 1000Å cannot be understood to be an obvious variation as it produces unexpected results. Reconsideration of claim 1 is requested.

Claims 2-7, 9 and 11-13 depend from claim 1, and, therefore, include at least its limitations. Each of these claims includes other limitations, which in combination with those of claim 1, are not shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on January 15, 2003:

Samuel H. Weiner

Name of applicant, assignee or Registered Representative

Signature

January 15, 2003

Date of Signature

Respectfully submitted,

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